REMARKS

Claims 1-16 were presented for examination and were pending in this application. In a Final Official Action dated April 20, 2004, claims 1-16 were rejected. Applicants thank Examiner for examination of the claims pending in this application and addresses Examiner's comments below. In addition, Applicants thank Examiner for taking the time to conduct the telephonic Examiner Interview of July 13, 2004. During the Interview, Applicants' representatives summarized some aspects of the claimed invention in view of representative claim 1 and discussed proposed amendments with Examiner Harkness. The Examiner indicated that the proposed amendments would seem to make the claims patentably distinguishable over the cited art but required further explanation in the Remarks section of this Amendment. This response incorporates a summary of the key points discussed during the Examiner Interview.

Applicants thank Examiner for withdrawal of the objection to the title.

Applicants submit an information disclosure statement herewith including a reference cited in the specification and incorporated by reference but not previously submitted for Examiner's review.

Applicants herein amend claims 1-5, 7 and 13-16. Claim 17-28 are added. Claims 2-5 and 13-16 have been amended to depend from new claim 17 and accordingly the recitation of the "state" element has been amended to properly depend from claim 17's "thread state" elements that provided the corresponding antecedent basis. Claim 1 has been amended as agreed with Examiner during the Examiner Interview to clarify the hardware-based approach of the present invention. These changes are not believed to introduce new matter, and their

entry is respectfully requested. The claims have been amended to expedite the prosecution of the application in a manner consistent with the Patent Office Business Goals, 65 Fed. Reg. 54603 (Sept. 8, 2000). In making these amendments, Applicants have not and do not narrow the scope of the protection to which Applicants consider the claimed invention to be entitled and do not concede that the subject matter of such claims was in fact disclosed or taught by the cited prior art. Rather, Applicants reserve the right to pursue such protection at a later point in time and merely seek to pursue protection for the subject matter presented in this submission.

Based on the above Amendments and the following Remarks, Applicants respectfully request that Examiner reconsider all outstanding objections and rejections, and withdraw them.

Response to Rejection Under 35 USC 102(b)

In the 4th paragraph of the Office Action, Examiner rejects claims 1-3, 5-9, and 13-16 under 35 USC § 102(b) as allegedly being anticipated by U.S. Patent No. 6,317,774 to Jones et al. ("Jones"). This rejection is now traversed.

Claim 1, as amended, recites:

> A computer based system for switching between program contexts comprising:
> an embedded pipelined processor capable of having a first program thread and a second program thread in an execution pipeline having a thread selection hardware;
> a first set of data storage devices capable of storing a first thread state of said embedded processor;
> a second set of data storage devices capable of storing a second thread state of said embedded processor; and
> a hardware thread scheduler for identifying which of said program threads said embedded processor executes and configurable to allocate available processing time of the embedded

pipelined processor among at least the first and second threads according to a fixed schedule;

wherein said thread selection hardware in the embedded pipelined processor switches between said first and second thread state after the end of the execution of a first program instruction in the first thread and before the beginning of the execution of a second program instruction.

The claimed system includes an embedded pipeline processor with thread selection hardware capable of having at least two program threads in a pipeline and a hardware thread scheduler that is configurable to allocate the processing time of the embedded processor according to a fixed schedule. Further, the embedded processor switches states of the threads between the execution of two consecutive instructions by means of the thread selection hardware, which switches from one set of memory devices to another each of which stores a thread state of the embedded processor. This hardware based switching is fast and done between consecutive instruction cycles, essentially in a "zero-time" manner (i.e., no instruction cycles are lost) thereby increasing computing speed. The fixed schedule is used to allocate computing time, for example a quantum, which for example provides a guaranteed timely processing of hard-real-time processes.

In contrast, Jones simply describes a multithreading operating system scheduling feature using a directed acyclic graph of nodes (col. 2, lines 51-54). The system in Jones includes a memory that "preferably contains an operating system, which preferably executes on the CPU 110 and includes the software scheduling facility (the scheduler)." (Jones 6:25-28). The scheduler of Jones is a software scheduler that resides within the operating system. See Jones Fig. 1 (_10 and _32). Jones describes the general operation of the system in which the scheduler executes as follows:

A thread is typically represented by a data structure called an execution context, which contains state information about the execution of

> the thread, such as register and stack contents. When the operating system suspends a thread in favor of the execution of another thread, *it copies the information from the registers and stack* to the thread's execution context. When the operating system subsequently reselects the thread for execution after suspending another thread, *it copies the information in the thread's execution context back to the actual registers and stack.* In this way, the thread continues executing with the same register and stack contents as when it was suspended.

Jones, 1:19-32 (emphasis added). Accordingly, the Jones reference discloses a software based scheduler that requires the copying of state information to and from a memory, which requires several instructions that execute over several instruction cycles.

This software based context switching is the conventional approach that the system of the present invention significantly improves by providing a hardware scheduler and thread selection hardware that switches between different sets of storage devices each of which stores a thread state of the embedded processor. The hardware based switching is done between instruction execution cycles, i.e., no instructions are required for copying to and from memory, because each thread has a dedicated set of memory devices to which the thread selection hardware switches according to the schedule.

Therefore, Jones does not describe an embedded processor with thread selection hardware as recited in claim 1. Rather, Jones describes an operating system scheduling software.

In a rejection under 35 U.S.C. §102, each and every claim element must be present in the applied reference. However, Examiner has failed to point out any prior "embedded pipeline processor" in Jones. Therefore, it is respectfully submitted that the rejection of claim 1 is improper and should be withdrawn.

New claim 17 recites the same type of "embedded pipelined processor with thread selection hardware ... wherein said thread selection hardware in the embedded pipelined processor switches from said first thread state to said second thread state between consecutive instruction cycles in response to the hardware thread scheduler identifying of which of said program threads said embedded processor executes."

As discussed above, Jones only describes as software scheduler that requires copying to and from memory as part of the context switching functions. Jones fails to teach or disclose the claimed hardware based context switching of claim 17.

As claims 2-16 are directly or indirectly dependent on claim 17, all arguments advanced above with respect to claims 1 and 17 are hereby incorporated so as to apply to claims 2-16.

Based on the above Amendment and Remarks, Applicants respectfully submit that for at least these reasons claims 1-3, 5-9, and 13-16 are patentably distinguishable over the cited reference. Therefore, Applicants respectfully request that Examiner reconsider the rejection, and withdraw it.

Response to Rejections Under 35 USC 103(a)

In the 16th paragraph of the Office Action, Examiner rejects claim 4 under 35 USC § 103(a) as allegedly being unpatentable over Jones in view of U.S. Patent No. 6,567,839 to Borkenhagen et al. ("Borkenhagen"). This rejection is respectfully traversed.

As described above with reference to claims 1 and 17, Jones fails to disclose at least "an embedded pipelined processor ... having thread a thread selection hardware." As claims

4 is dependent on claim 17, all arguments advanced above with respect to claims 1 and 17 are hereby incorporated so as to apply to claim 4.

Borkenhagen discloses a thread switch control in a multithreaded processor system that can switch between threads "as a result of any or a combination of several events." (Borkenhagen, col. 6:28-29.) The system of Borkenhagen does not operate according to any schedule, it is event driven. Id. Further, with respect to context switching, it includes the conventional "latency and performance penalties associated with switching threads." (Borkenhagen, col. 15:37-38).

> In the multithreaded processor in the preferred embodiment described herein, this latency includes the time required to complete execution of the current thread to a point where it can be interrupted and correctly restarted when it is next invoked, *the time required to switch the thread-specific hardware facilities from the current thread's state to the new thread's state*, and the time required to restart the new thread and begin its execution.

Borkenhagen, col. 15:38-46 (emphasis added).

Consequently, Borkenhagen also fails to disclose the embedded processor of claims 1 and 17 "wherein said thread selection hardware in the embedded pipelined processor switches from said first thread state to said second thread state between consecutive instruction cycles in response to the hardware thread scheduler identifying of which of said program threads said embedded processor executes."

Based on the above Amendment and Remarks, Applicants respectfully submit that for at least these reasons claim 4 is patentably distinguishable over the cited references, both alone and in combination. Therefore, Applicants respectfully request that Examiner reconsider the rejection, and withdraw it.

In the 18th paragraph of the Office Action, Examiner rejects claim 10-12 under 35 USC § 103(a) as allegedly being unpatentable over Jones in view of U.S. Patent No. 6,026,503 to Gutgold et al. ("Gutgold"). This rejection is respectfully traversed.

As described above with reference to claims 1 and 17, Jones fails to disclose at least "an embedded pipelined processor ... having thread a thread selection hardware." As claims 10-12 are dependent on claim 17, all arguments advanced above with respect to claims 1 and 17 are hereby incorporated so as to apply to claims 10-12.

Further, Gutgold also fails to disclose as least this element. Gutgold describes a "device and method foe interactively debugging a system controlled by a microprocessor." (Abstract). Gutgold teaches the connection of a debugging device to a microprocessor/bus interface to monitor the exchange of signals. (col. 3, lines 20-22). There is no mention or suggestion of "an embedded pipelined processor ... having a thread selection hardware" as claimed in the present invention.

Therefore, based on the above Amendment and Remarks, Applicants respectfully submit that for at least these reasons claims 10-12 are patentably distinguishable over the cited references, both alone and in combination. Therefore, Applicants respectfully request that Examiner reconsider the rejection, and withdraw it.

Conclusion

In sum, Applicants respectfully submit that claims 1 through 28, as presented herein, are patentably distinguishable over the cited references. Therefore, Applicants request reconsideration of the basis for the rejections to these claims and request allowance of them.

In addition, Applicants respectfully invite Examiner to contact Applicants' representative at the number provided below if Examiner believes it will help expedite furtherance of this application.

Respectfully Submitted,
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